IN THE CLAIMS

Please cancel claims 3 and 6 without prejudice. Claims 16-25 are new.

Please amend the following claims which are pending in the present application:

1. (Currently amended) A combination wafer ~~or microelectronic die~~, comprising:

a substrate;

a plurality of electronic elements formed in or on the substrate;

a first set of alternating dielectric layers and layers of metal lines on the substrate, the first set having a first guard ring trench therein with a first width;

a first guard ring layer formed on surfaces of the first guard ring trench;

a second set of alternating dielectric layers and layers of metal lines on the first set, the second set having a second guard ring trench therein, above the first guard ring trench and having a second width which is wider than the first width; [[and]]

a second guard ring layer formed on surfaces of the second guard ring trench[[.]];

a third set of alternating dielectric layers and layers of metal lines on the second set, the third set having a third guard ring trench therein, above the second guard ring trench and having a third width which is wider than the second width; and

a third guard ring layer formed on surfaces of the third guard ring trench.

2. (Currently amended) The combination wafer ~~or microelectronic die~~ of claim 1, wherein:

(i) the first guard ring layer is partially formed on a top surface of a layer of the first set; and

(ii) the second guard ring layer is partially formed on a top surface of the first guard ring layer where the first guard ring layer is formed on the top surface of the layer of the first set.

3. (Cancelled)

4. (Currently amended) The combination wafer ~~or microelectronic die~~ of claim 1, wherein lower ones of the dielectric layers of the first set include carbon and an upper one of the dielectric layers of the first set is made of a different material than the layers that include carbon.

5. (Currently amended) The combination wafer ~~or microelectronic die~~ of claim 4, wherein the upper dielectric layer of the first set includes substantially no carbon.

6. (Cancelled)

7. (Currently amended) A combination wafer ~~or microelectronic die~~, comprising:

a substrate;

a plurality of electronic elements formed in or on the substrate;

a first set of alternating dielectric layers and layers of metal lines on the substrate, the first set having a first guard ring trench therein with a first width;

a first guard ring layer formed on surfaces of the first guard ring trench, including partially on a top surface of an upper layer of the first set;

a second set of alternating dielectric layers and layers of metal lines on the first set, the second set having a second guard ring trench therein, above the first guard ring trench and having a second width which is wider than the first width;

a second guard ring layer formed on surfaces of the second guard ring trench, including partially on a top surface of the first guard ring layer where the first guard ring layer is formed on the top surface of the upper layer of the first set and partially on a top surface of an upper layer of the second set;

a third set of alternating dielectric layers and layers of metal lines on the second set, the third set having a third guard ring trench therein, above the second guard ring trench and having a third width which is wider than the second width; and

a third guard ring layer formed on surfaces of the third guard ring trench, including partially on a top surface of the second guard ring layer where the

second guard ring layer is formed on the top surface of the upper layer of the second set and partially on a top surface of an upper layer of the third set.

8. (Currently amended) The combination wafer ~~or microelectronic die~~ of claim 7, wherein:

(i) lower ones of the dielectric layers of the first set include carbon and an upper one of the dielectric layers of the first set is made of a different material than the layers that include carbon; and

(ii) lower ones of the dielectric layers of the second set include carbon and an upper one of the dielectric layers of the second set is made of a different material than the layers that include carbon.

9. (Currently amended) The combination wafer ~~or microelectronic die~~ of claim 8, wherein:

(i) wherein the upper dielectric layer of the first set includes substantially no carbon; and

(ii) wherein the upper dielectric layer of the second set includes substantially no carbon.

10. (Currently amended) A combination wafer ~~or microelectronic die~~, comprising:

a substrate;

a plurality of electronic elements formed in or on the substrate;

~~a plurality of alternating~~ at least three dielectric layers [[and]] alternated by layers of metal lines on the substrate, ~~a plurality of~~ at least three successively wider guard ring trenches respectively being formed above one another in the ~~alternating~~ respective dielectric layers; and

at least [[one]] three guard ring layers formed on surfaces of the respective guard ring trenches.

11. (Currently amended) The combination wafer ~~or microelectronic die~~ of claim 10, wherein more guard ring layers are formed on surfaces of a lower guard ring trench than on surfaces of an upper guard ring trench.

12. (Currently amended) The combination wafer ~~or microelectronic die~~ of claim 10, wherein each guard ring trench is substantially the same width into at least two of the dielectric layers.

13. (Currently amended) A method of making a combination wafer, comprising:

forming a first ground ring trench having a first width into a first set of alternating dielectric layers and layers of metal lines on a substrate having a plurality of electronic elements formed therein or thereon;

forming a first guard ring layer on surfaces of the first guard ring trench;

forming a second guard ring trench having a second width which is more than the first width above the first guard ring trench into a second set of alternating dielectric layers and layers of metal lines on the first set; [[and]]

forming a second guard ring layer on surfaces of the second guard ring trench[[.]];

forming a third guard ring trench having a third width which is more than the second width above the second guard ring trench into a third set of alternating dielectric layers and layers of metal lines on the second set; and

forming a third guard ring layer on surfaces of the third guard ring trench.

14. (Original) The method of claim 13, further comprising:

forming the second set of layers after the first guard ring layer is formed.

15. (Original) The method of claim 13, wherein:

(i) the first guard ring layer is partially formed on a top surface of a layer of the first set; and

(ii) the second guard ring layer is partially formed on a top surface of the first guard ring layer where the first guard ring layer is formed on the top surface of the layer of the first set.

16. (New) A microelectronic die, comprising:

a substrate;

a plurality of electronic elements formed in or on the substrate;

a first set of alternating dielectric layers and layers of metal lines on the substrate, the first set having a first guard ring trench therein with a first width;

a first guard ring layer formed on surfaces of the first guard ring trench;

a second set of alternating dielectric layers and layers of metal lines on the first set, the second set having a second guard ring trench therein, above the first guard ring trench and having a second width which is wider than the first width;

a second guard ring layer formed on surfaces of the second guard ring trench;

a third set of alternating dielectric layers and layers of metal lines on the second set, the third set having a third guard ring trench therein, above the second guard ring trench and having a third width which is wider than the second width; and

a third guard ring layer formed on surfaces of the third guard ring trench.

17. (New) The combination wafer of claim 16, wherein:

(i) the first guard ring layer is partially formed on a top surface of a layer of the first set; and

(ii) the second guard ring layer is partially formed on a top surface of the first guard ring layer where the first guard ring layer is formed on the top surface of the layer of the first set.

18. (New) The combination wafer of claim 16, wherein lower ones of the dielectric layers of the first set include carbon and an upper one of the dielectric layers of the first set is made of a different material than the layers that include carbon.

19. (New) The combination wafer of claim 18, wherein the upper dielectric layer of the first set includes substantially no carbon.

20. (New) A microelectronic die, comprising:

a substrate;

a plurality of electronic elements formed in or on the substrate;

a first set of alternating dielectric layers and layers of metal lines on the substrate, the first set having a first guard ring trench therein with a first width;

a first guard ring layer formed on surfaces of the first guard ring trench, including partially on a top surface of an upper layer of the first set;

a second set of alternating dielectric layers and layers of metal lines on the first set, the second set having a second guard ring trench therein, above the first guard ring trench and having a second width which is wider than the first width;

a second guard ring layer formed on surfaces of the second guard ring trench, including partially on a top surface of the first guard ring layer where the first guard ring layer is formed on the top surface of the upper layer of the first set and partially on a top surface of an upper layer of the second set;

a third set of alternating dielectric layers and layers of metal lines on the second set, the third set having a third guard ring trench therein, above the second guard ring trench and having a third width which is wider than the second width; and

a third guard ring layer formed on surfaces of the third guard ring trench, including partially on a top surface of the second guard ring layer where the second guard ring layer is formed on the top surface of the upper layer of the second set and partially on a top surface of an upper layer of the third set.

21. (New) The microelectronic die of claim 20, wherein:

(i) lower ones of the dielectric layers of the first set include carbon and an upper one of the dielectric layers of the first set is made of a different material than the layers that include carbon; and

(ii) lower ones of the dielectric layers of the second set include carbon and an upper one of the dielectric layers of the second set is made of a different material than the layers that include carbon.

22. (New) The microelectronic die of claim 21, wherein:

(i) wherein the upper dielectric layer of the first set includes substantially no carbon; and

(ii) wherein the upper dielectric layer of the second set includes substantially no carbon.

23. (New) A microelectronic die, comprising:

a substrate;

a plurality of electronic elements formed in or on the substrate;

at least three dielectric layers alternated by layers of metal lines on the substrate, at least three successively wider guard ring trenches respectively being formed above one another in the respective dielectric layers; and

at least three guard ring layers formed on surfaces of the respective guard ring trenches.

24. (New) The microelectronic die of claim 23, wherein more guard ring layers are formed on surfaces of a lower guard ring trench than on surfaces of an upper guard ring trench.

25. (New) The microelectronic die of claim 24, wherein each guard ring trench is substantially the same width into at least two of the dielectric layers.